PATENT

I hereby certify that on the date, specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner of Patents, Washington, DC 20231.

May 23, 2001
Date

Ayesha S. Wilks

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	: James R. Peterson and William Radke	Attorney Docket No.:	500689.01
Serial No.	: 09/602,901	Group Art Unit	: 2776
Filed	: June 23, 2000	Examiner	: Not Yet Assigned
Title	: APPARATUS AND METHOD FOR DYNAMICALLY DISABLING FAULTY EMBEDDED MEMORY IN A GRAPHIC PROCESSING SYSTEM		

PRELIMINARY AMENDMENT

Commissioner of Patents
Washington, D.C. 20231

Sir:

Please amend the above-identified application as follows:

In the Specification:

Please replace the paragraph beginning on page 9, line 1, with the following rewritten paragraph:

--Figure 4 illustrates a distributed memory controller memory subsystem 400 that may be substituted into a graphics processing system. A more detailed description of a similar memory subsystem is provided in Patent Application No. 09/603,158, filed June 23, 2000, which is incorporated herein by reference. To summarize, the memory subsystem 400 includes two memory controllers 402 and 422 coupled together through a memory controller bus 216. The